Fig. 1 PRIOR ART

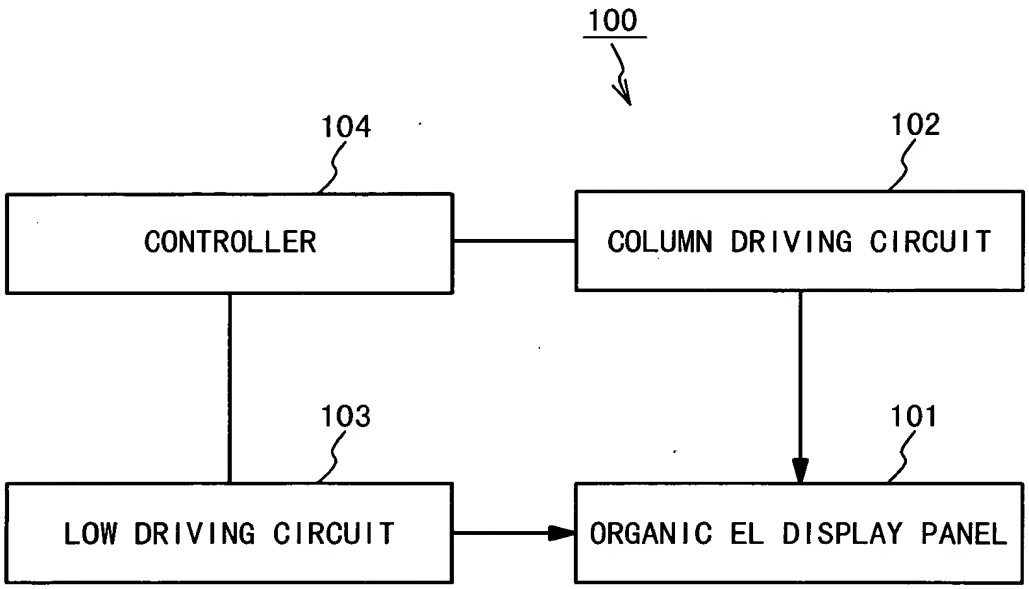


Fig. 2

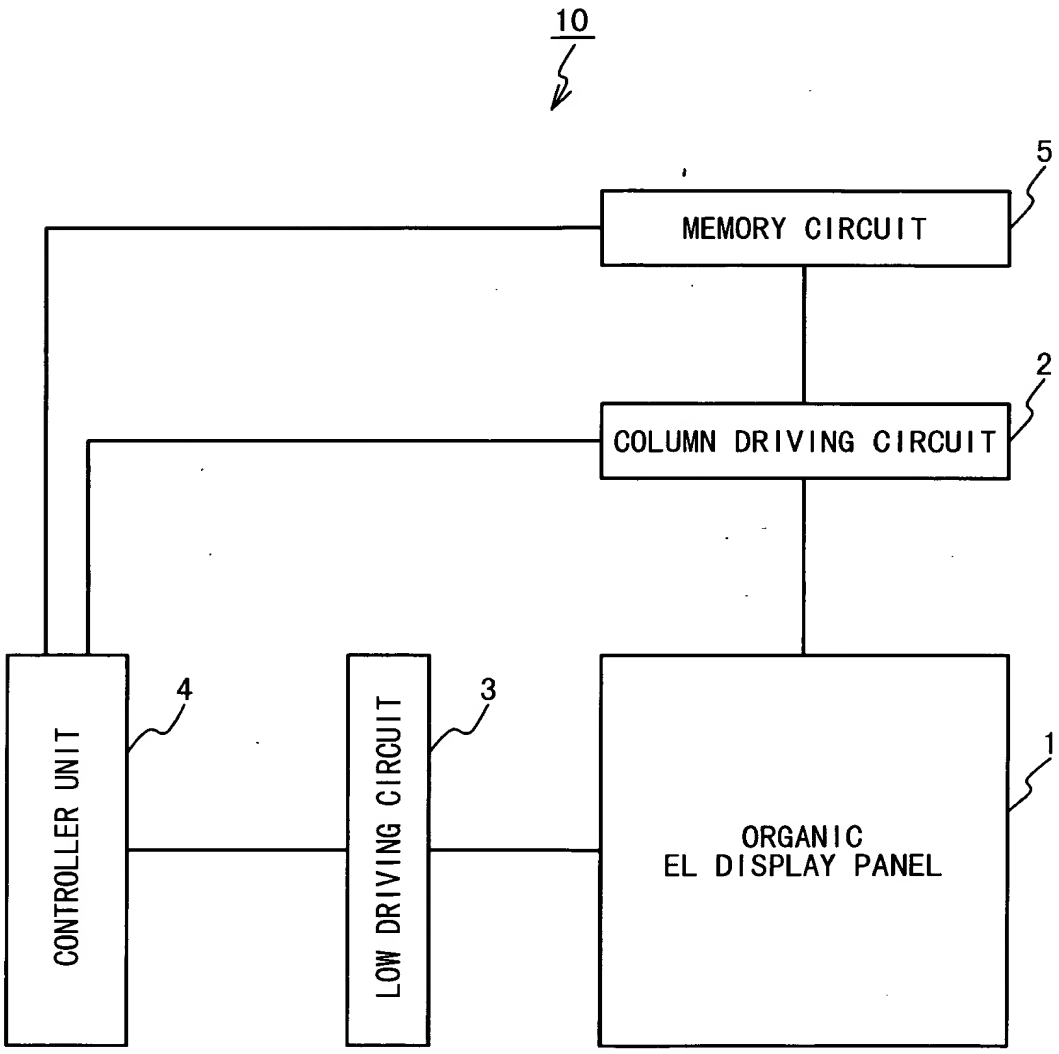

10
5
MEMORY CIRCUIT
2
COLUMN DRIVING CIRCUIT
4
CONTROLLER UNIT
3
LOW DRIVING CIRCUIT
1
ORGANIC
EL DISPLAY PANEL

Fig. 3

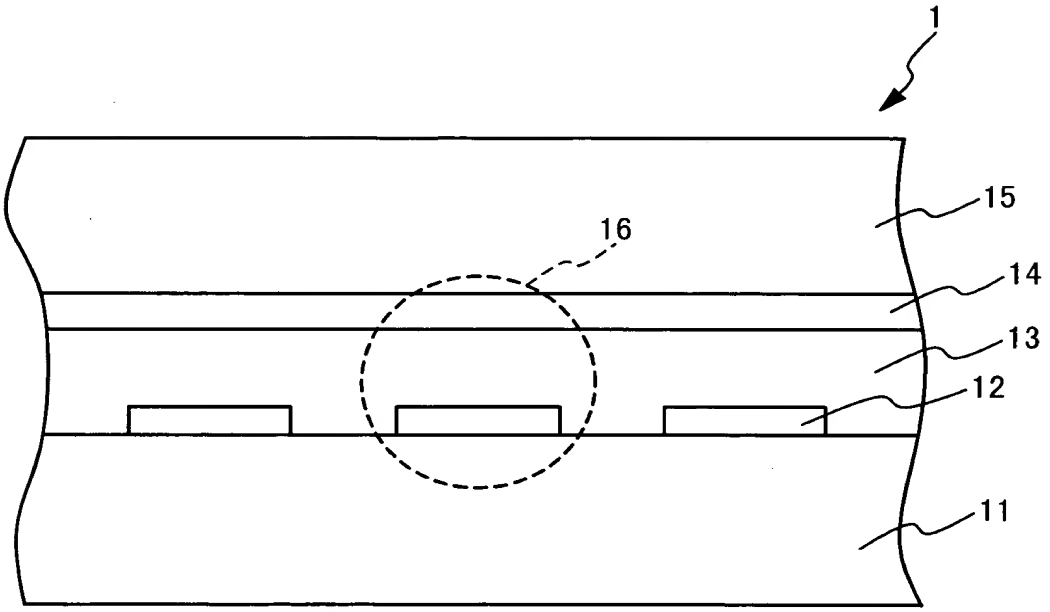


Fig. 4

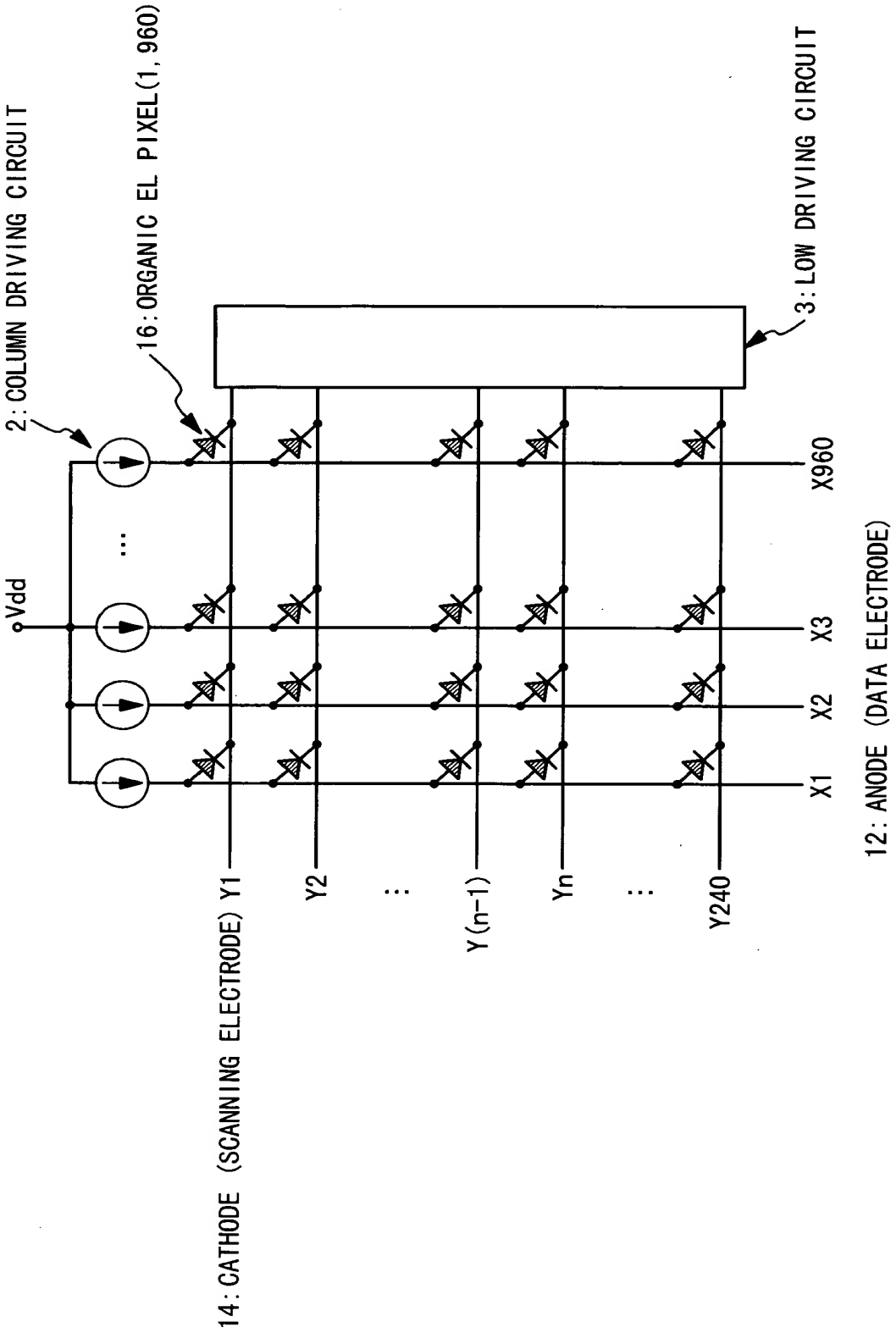

2: COLUMN DRIVING CIRCUIT
16: ORGANIC EL PIXEL(1, 960)
3: LOW DRIVING CIRCUIT
Vdd
X960
X3
X2
X1
Y1
Y2
Y(n-1)
Yn
Y240
14: CATHODE (SCANNING ELECTRODE)
12: ANODE (DATA ELECTRODE)

Fig. 5

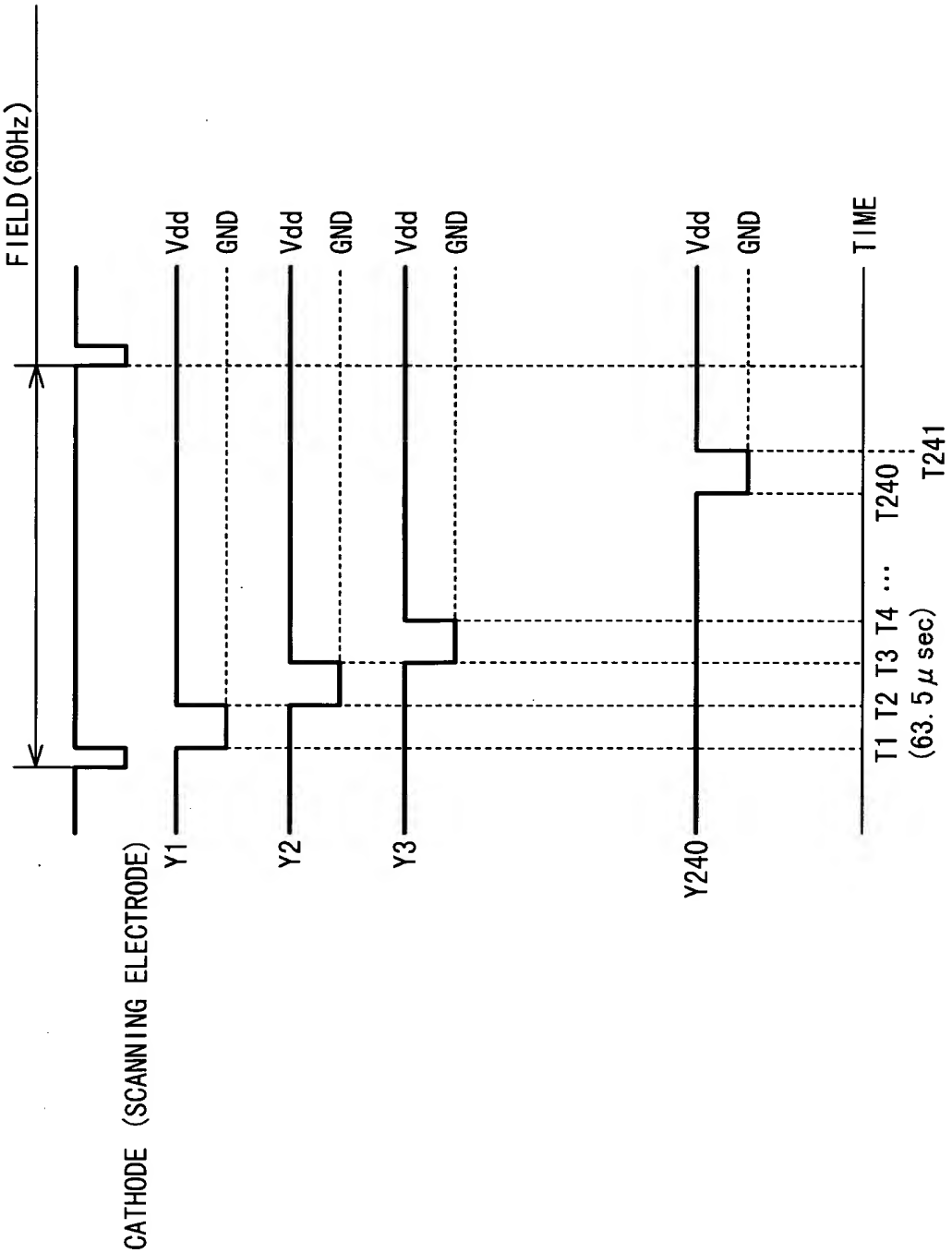

FIELD(60Hz)
Vdd
GND
Vdd
GND
Vdd
GND
Vdd
GND
TIME
T1 T2 T3 T4 ··· T240 T241
(63.5 μ sec)
CATHODE (SCANNING ELECTRODE)
Y1
Y2
Y3
Y240

Fig. 6A

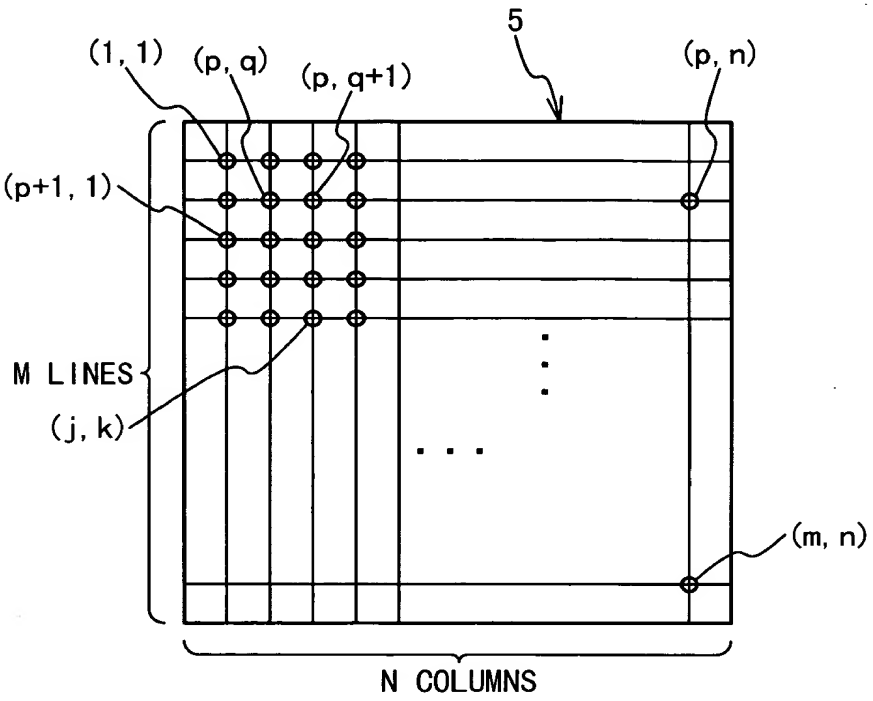

5
(1, 1)
(p, q)
(p, q+1)
(p, n)
(p+1, 1)
M LINES
(j, k)
(m, n)
N COLUMNS

Fig. 6B

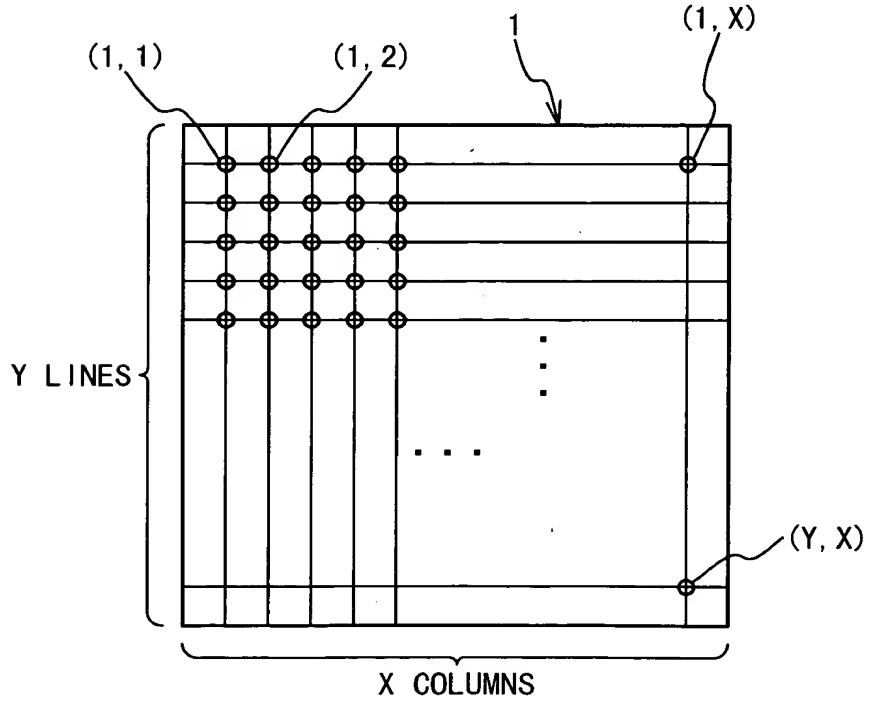
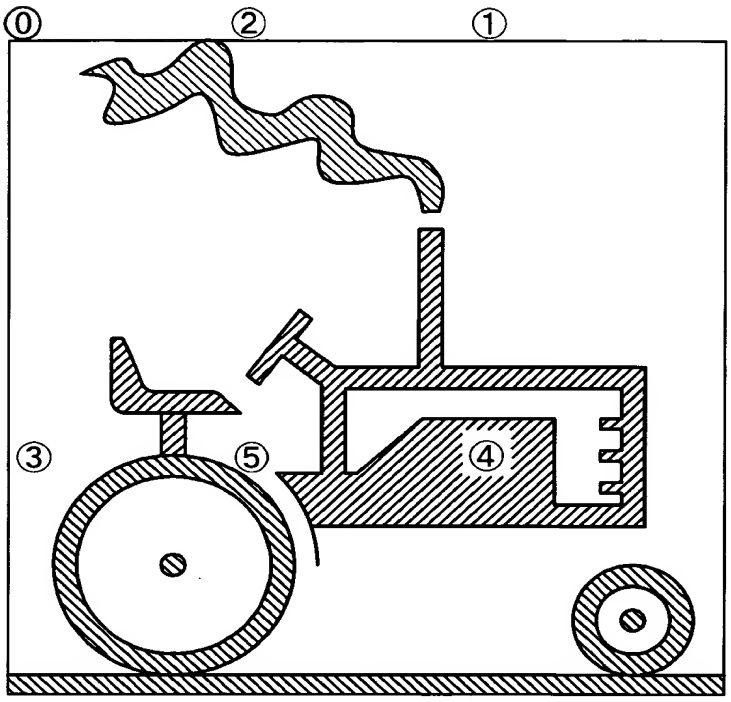
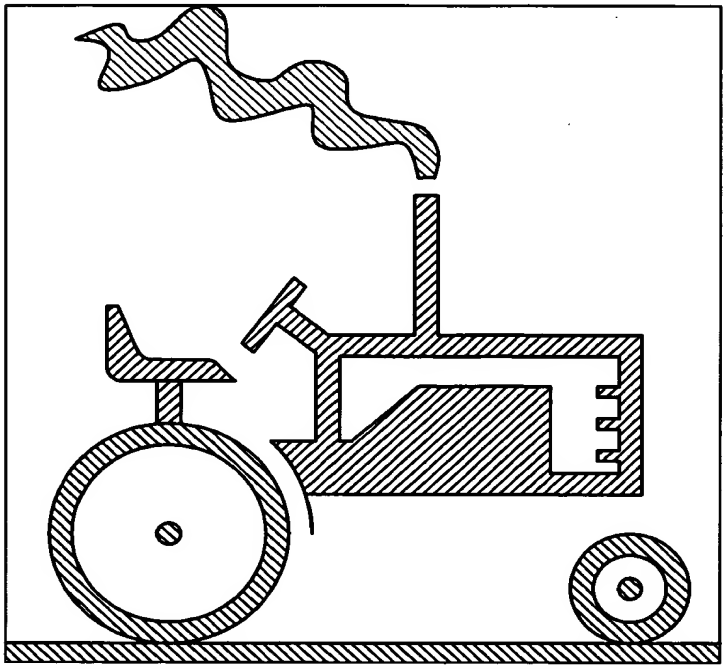

1
(1, X)
(1, 1)
(1, 2)
Y LINES
(Y, X)
X COLUMNS

Fig. 7



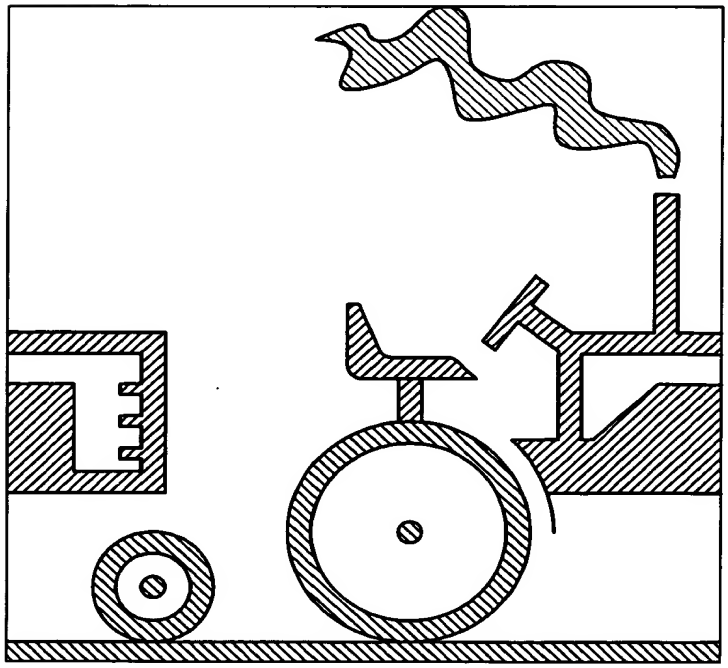
THE START POSITION IN RAM MOVES OR SHIFT(0→1→2→3→4→5)

Fig. 8A



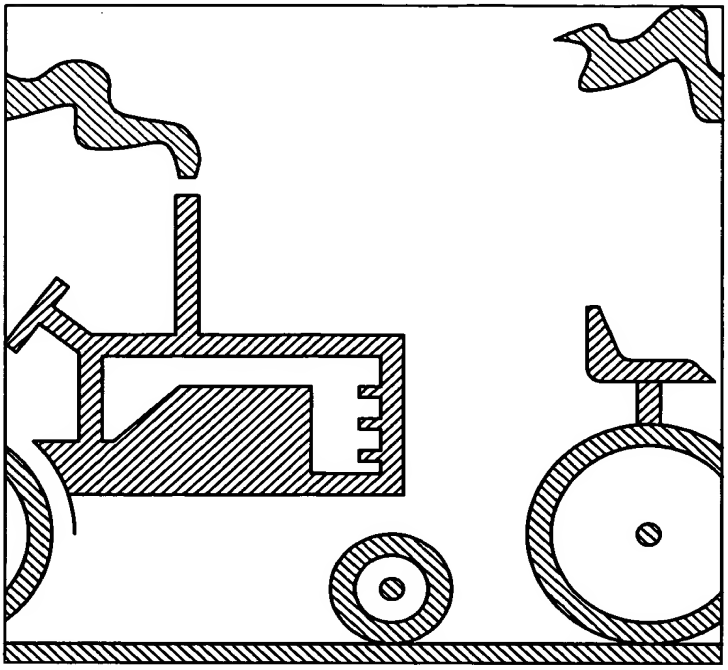
ORIGINAL DISPLAY

Fig. 8B



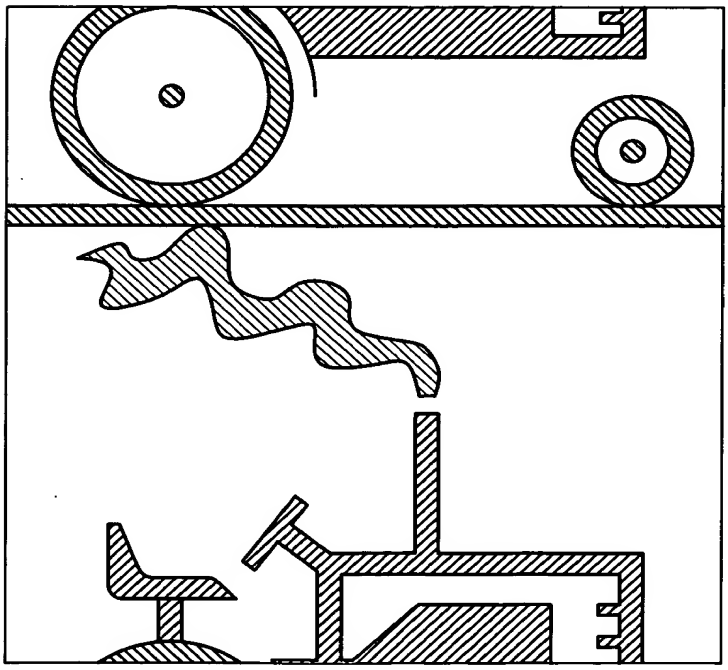
ZIGZAG1

Fig. 9A



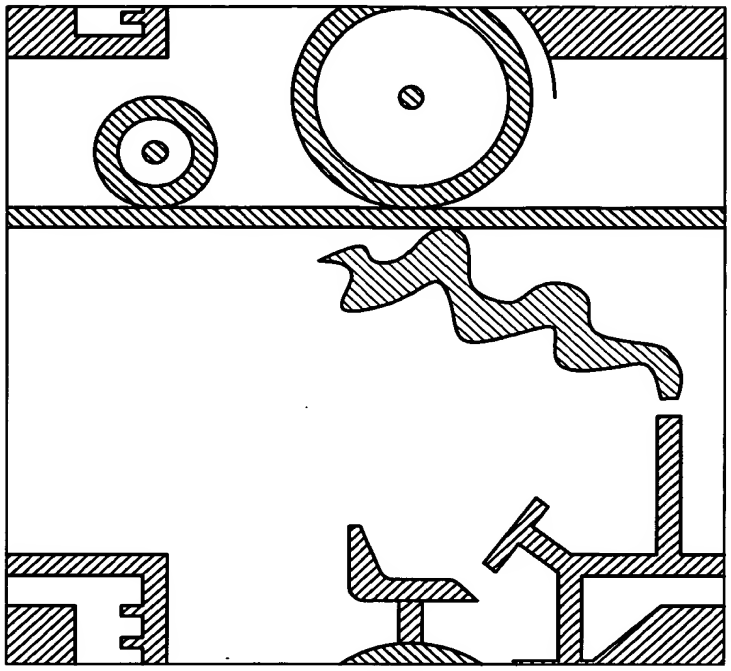
ZIGZAG2

Fig. 9B



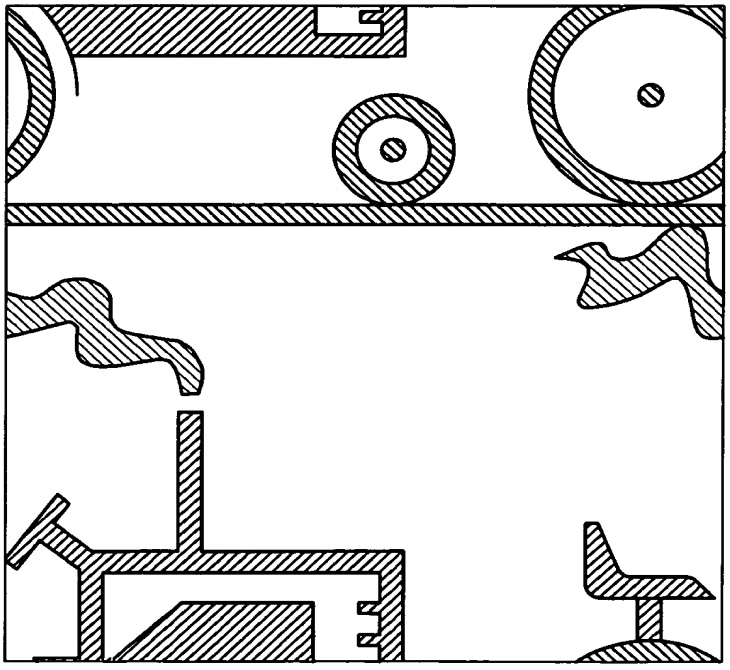
ZIGZAG3

Fig. 10A



ZIGZAG4

Fig. 10B



ZIGZAG5

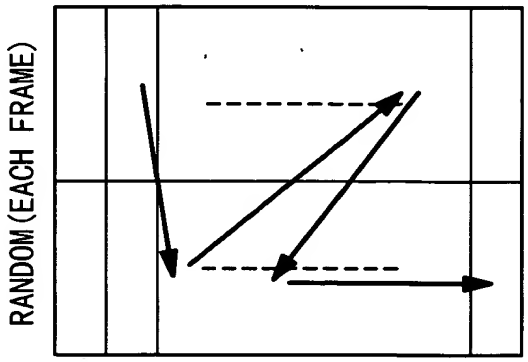


Fig. 11D

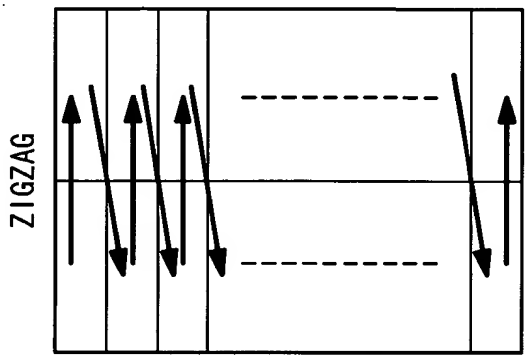


Fig. 11C

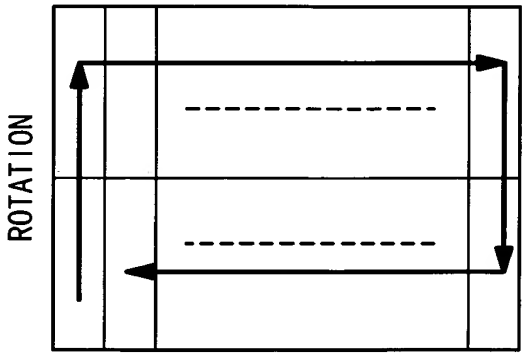


Fig. 11B

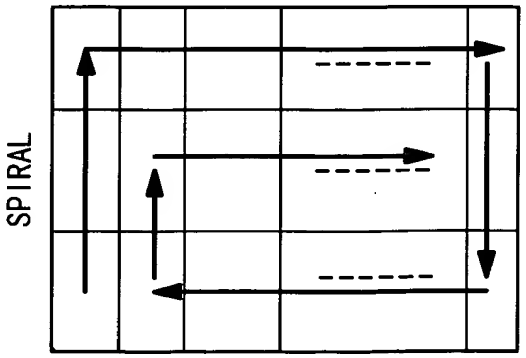


Fig. 11A